Claims

What is claimed is:

1. A 3-D graphics chip having embedded DRAM buffers, the chip comprising:

an embedded DRAM partitioned into drawing buffers;

a 3-D drawing engine configured to concurrently access the embedded drawing buffers for providing rendered 3-D drawing information; and

output means permitting the graphics chip to output the rendered 3-D drawing information.

2. The 3-D graphics chip as set forth in Claim 1, further including the drawing engine implementing concurrent drawing processes, the drawing processes being interrelated in a predetermined manner.

3. The 3-D graphics chip as set forth in Claim 2, further including a plurality of independent read FIFO's and write FIFO's used by the concurrent drawing processes to access the embedded buffers.

4. The 3-D graphics chip as set forth in Claim 3, further including an access priority engine, communicating with all FIFO's needing access to a given drawing buffer, and granting access priority in a dynamic manner to each such FIFO, one-at-a-time, thereby insuring that each concurrent drawing process obtains needed buffer access.

5. The 3-D graphics chip as set forth in Claim 4, further including a wide bandwidth access bus for connecting a FIFO having the granted access priority with the embedded DRAM.

6. The 3-D graphics chip as set forth in Claim 1, further including the embedded DRAM being arranged in at least two independent memory banks, and each memory bank having a separate wide bandwidth access bus, and each access bus having a corresponding access priority engine communicating with the FIFO's.

7. The 3-D graphics chip as set forth in Claim 6, further including a plurality of programmable switches, and each FIFO being connectable to a selected access bus and a corresponding access priority engine via the programmable switches.

8. The 3-D graphics chip as set forth in Claim 7, further including at least two drawing buffers located within a single memory bank, and the FIFO's for the corresponding drawing processes being connected to the access bus and the priority engine for said memory bank via the programmable switches.

9. The 3-D graphics chip as set forth in Claim 7, further including means permitting a host device to program said switches for configuring the drawing processes via FIFO's to drawing buffers in selected memory banks.

10. The 3-D graphics chip as set forth in Claim 4, further including each FIFO having its own address register and offset register permitting each FIFO to access the entire address space of the embedded DRAM.

11. The 3-D graphics chip as set forth in Claim 1, further including a separate external memory access bus permitting at least one drawing buffer to be located in an external memory.

12. The 3-D graphics chip as set forth in Claim 1, further including means permitting a host device to initialize the contents of a drawing buffer.

13. The 3-D graphics chip as set forth in Claim 1, further including means permitting a host device to initialize the 3-D drawing engine.

14. A 3-D graphics system using embedded buffers and fabricated on a single substrate, the system comprising:

an embedded DRAM partitioned into drawing buffers;

a 3-D drawing engine implementing concurrent 3-D drawing processes using and updating drawing information stored in the drawing buffers;

a plurality of independent read FIFO's and write FIFO's permitting the concurrent drawing processes to access the contents of the drawing buffers;

a wide bandwidth access bus for connecting the independent FIFO's with the embedded DRAM;

the concurrent drawing processes being interrelated such that the buffer contents are acted upon in a predefined read sequence and such that updated drawing information is produced in a predefined write sequence;

the concurrent drawing processes withdrawing the accessed drawing information from the read FIFO's according to the predefined read sequence;

the concurrent drawing processes placing updated drawing information into the write FIFO's according to the predefined write sequence;

each read FIFO independently filling with accessed drawing information at a rate permitted by the wide-bandwidth access bus and competing FIFO's;

each write FIFO independently emptying of updated drawing information at a rate permitted by the wide-bandwidth access bus and competing FIFO's; and

an access priority engine communicating with each read FIFO and with each write FIFO for resolving drawing buffer access competition by permitting each FIFO to use the wide-bandwidth access bus for accessing the embedded drawing buffers, and to insure that no FIFO is denied needed access,

whereby the 3-D graphics system throughput is maximized without incurring I/O pin limitations required for wide-bandwidth external drawing buffers.

15. A 3-D graphics system using embedded buffers and fabricated on a single substrate, the system comprising:

a 3-D drawing engine implementing concurrent 3-D drawing processes;

first and second embedded DRAM used for drawing buffers;

a plurality of read FIFO's used by the concurrent drawing processes for fetching information from the drawing buffers;

a plurality of write FIFO's used by the concurrent drawing processes for storing information into the drawing buffers;

a plurality of programmable switches configurable for connecting the FIFO's for a specific drawing process to a selected embedded DRAM;

each DRAM having a corresponding access priority engine for determining access priority among FIFO's competing for access to the corresponding DRAM.

16. The 3-D graphics system as set forth in Claim 15, further including external bus – means for connecting FIFO's to an external memory for implementing an external memory drawing buffer.

17. The 3-D graphics system as set forth in Claim 16, wherein the external bus means includes an access priority engine for determining access priority among FIFO's competing for access to the external memory.

18. The 3-D graphics system as set forth in Claim 15, further including means permitting a host device to program the configurable switches for connecting the FIFO's to selected drawing buffers.

19. The 3-D graphics system as set forth in Claim 15, further including means permitting a host device to initialize the contents of a drawing buffer.

20. The 3-D graphics system as set forth in Claim 15, further including means permitting a host device to store drawing engine control information in a portion of one embedded DRAM and defining a control buffer.

21. The 3-D graphics system as set forth in Claim 20, further including the 3-D drawing engine responsive to control information stored in the control buffer.

22. The 3-D graphics system as set forth in Claim 20, wherein the drawing engine control information defines a display list buffer storing geometric attributes of 3-D graphics.